CSPs USE CHALLENGES

- Maturity
  - Cost: SLICC vs. JACS-Pak
  - Licensees with different materials, processes
  - Materials/Deign
    - Continuos changes
- Availability
  - ICs in CSP format
- Reliability
  - Some data screening for packages
  - Some assembly reliability
- Supplier desire on **reliability**
  - **Trust what they say!**

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CSPs RELIABILITY -1

- Applications
  - Low, Medium, and High I/Os
- Testing Modules
  - Daisy chain packages less critical
  - Test and burn-in socket availability for active die
- Design Guidelines CSP
  - Not available
- Standards
  - Construction, Pitches, Solder balls

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CSPs RELIABILITY -2

- PWB Materials
  - Low to medium I/Os
    - Standard
  - High I/O
    - Microvia (build up) technology
- Process Requirements
  - Experience of using CSPs in SMT line
  - Mixed technology
    - Routability, Thermal mass, Cleaning, etc.
  - Underfill, etc.

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CSPs RELIABILITY -3

- Reliability
  - Aerospace
    - Stringent requirements and long time
  - Commercial
    - Less stringent and short time
- Inspection
  - Hidden solders not inspectable
- Rework
  - Miniature package
    - Improved tool or modified procedures
  - Underfill

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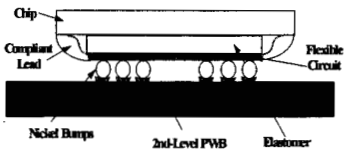
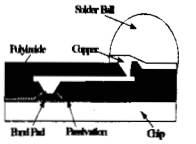
CSP Board Reliability Types

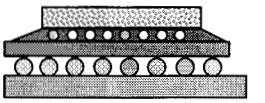
- CTE Absorbed CSP
  - Use of TAB
  - Solder joint low strain
    - No underfill
  - Reliability limit
    - TAB, material, etc. Data from manufacturer & user



- Extreme CTE Mismatch
  - Wafer level
    - Same as flip chip with slight improvement
    - Underfill requirement



- Ceramic package with rigid interposer
  - Non-wafer level
    - Improved reliability to CBGA version



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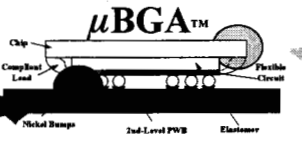
CSP Reliability Prediction

W/O Consideration for Failure Mechanisms



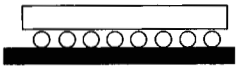
Prediction

FR-4	Flex	
7,130 Cycles	**13,14**	**(-55°C/125°C)**
15,190	27,820	(-55°C/85°C)

Data Source: R. Larmouth, SMI '97

Test Results
1,000 ~ Intel
600 ~ Motorola
500 ~ Gintic

FCOB/F



FR-4	Flex	
77	**178**	**(-55°C/125°C)**

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JPL AIP
QA Section

NASA Code Q, AE

JPL SMT Program
'92 - '97

BGA CONSORTIUM
'95-'98

'97-'00
Consortium
MicrotypeBGA

CSP CONSORTIUM
'98-'01

Rajeev Ghaffarian

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Consortium
MicrotypeBGA

Program Objectives

Demonstrate controls, quality, and reliability of Microtype Ball Grid Array interconnects

&

Support the development of industrial infrastructure in product assurance

- Inspection methodology development, especially for assembly level
- Optimal package type configuration
- Reliability characterization
  - Package type, I/O, and Environmental dependency
- Reworking techniques

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Conclusions-BGA

- CBGA 625 I/Os were first to fail under different cycling ranges than
  - CBGA 361
  - SBGA 560, SBGA 352, OMPAC 352, and PBGA 256 when cycled to different temperature ranges
- PBGAs 313 I/O, depopulated full arrays, were first among the PBGAs to fail
- SBGA 352 with no solder balls under the die showed much higher cycles to failure than the PBGA 313

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Conclusions-CSP

- **CSPs alignment characteristics**
  - Depend on package type, ball material, weight of package
  - 30 trial assemblies of 46 I/O, no defect
- **Mixed Technology**
  - Solder volume not optimum for leadless the most needed
- **Trial TV Cycling Results**
  - Low I/O wafer had poor quality
  - Double sided leadless was first to failure

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Future Activities

- Package aging test results
- Complete 1 50 additional TVs with different PWB surface finishes
- Extensive thermal and mechanical evaluation of assemblies
- **CSP Consortium- Mixed technology & active die including CSP, flip chip, BGA**
- Guidelines documents
  - for BGA: http://www.ITRI.org

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Acknowledgments

NASA, Code Q, AE
AIP RTOPs
(Advanced Interconnect Program)

Also, in-kind contributions and cooperative efforts of

BGA CONSORTIUM

CSP CONSORTIUM

Consortium team members and others

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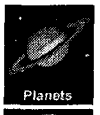
DAA

Jet Propulsion Laboratory
National Aeronautics & Space Administration
California Institute of Technology



Assessment of Strengths & Weaknesses for Major IC Packages

by

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Outline

- Package Miniaturization Trends
- BGA vs. QFP
- CSP
  - CSP vs. Flip Chip
  - Grid CSP vs. leads/no leads
  - Implementation challenges
- Thermal Cycling Fatigue
  - Optimum CTE mismatch
  - Reliability of BGA vs. QFP
  - Reliability of CSPs
- Conclusions

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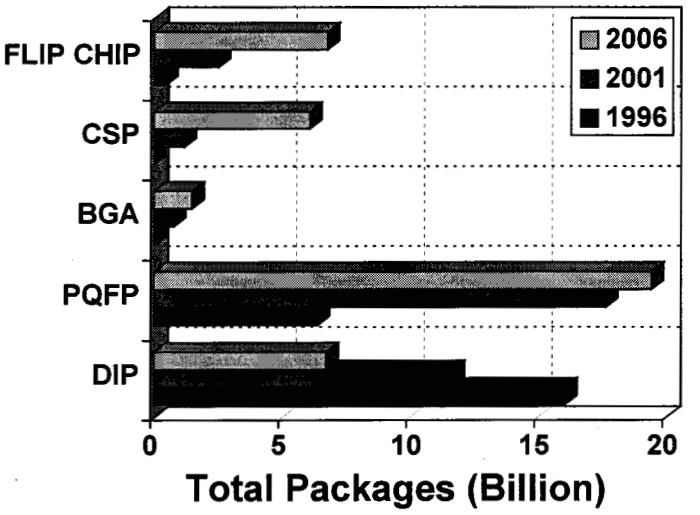
Package Use for Next Decade



Adapted from BPA, SMI '97

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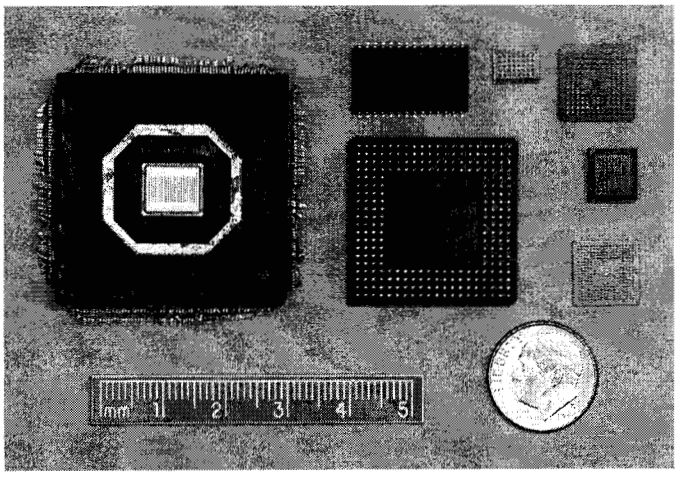
ADVANCED IC PACKAGES



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BGA vs QFP

- Advantages
  - Capable of high pin counts
  - Manufacturing robustness
  - Higher package densities
  - Faster circuitry speed than QFP
  - Better heat dissipation
- Challenges
  - **Inspection**
  - Multiple processes and double sided assemblies
  - Routing for high pin count
  - Rework, especially individual balls

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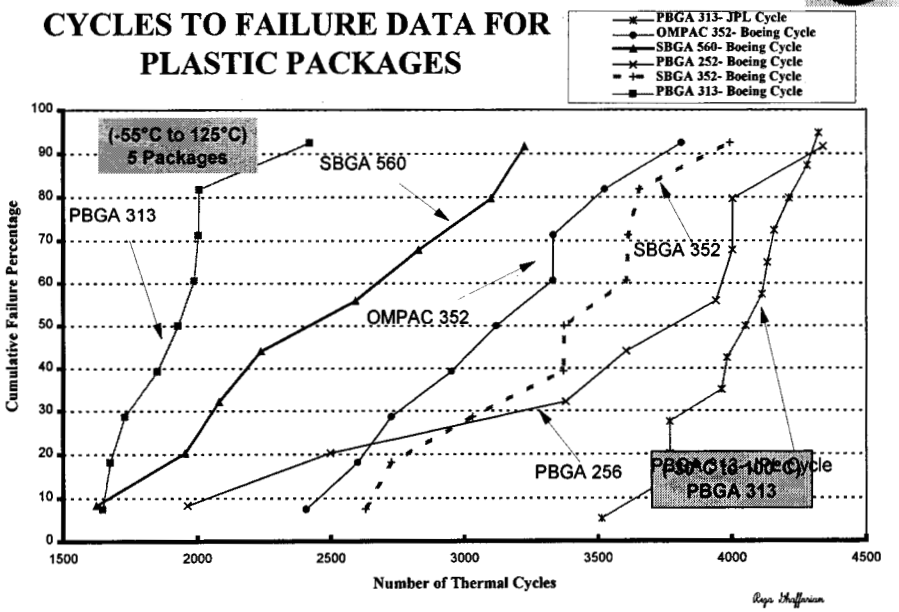
CYCLES TO FAILURE DATA FOR PLASTIC PACKAGES



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Chip Scale Package Definition

- Near bare die size
  - 1.2 of die perimeter or 1.5 of area
- **Industry definition!**
  - Any package with pitch lower than previous version!
- Package purposes
  - Balls/leads compatibility with the PWB reflow
    - *-Aluminum pads on die are not reflow compatible*
  - Die tight pitch redistribution to the PWB norm
  - Die protection from physical and alpha radiation
  - Thermal dissipation path and ease of testability

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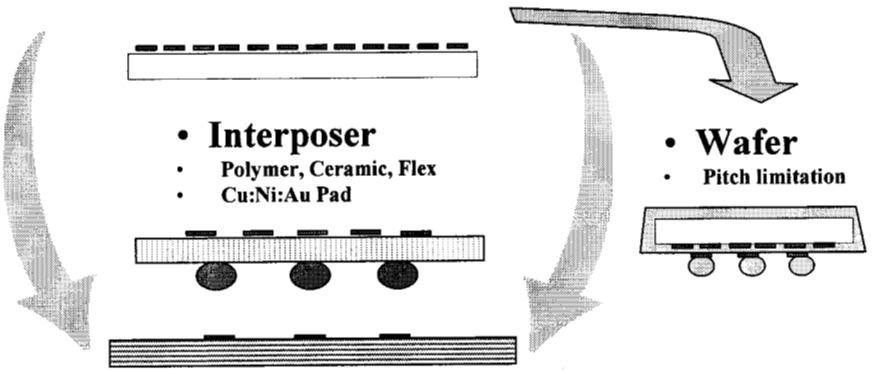
CSPs Concepts

- **Die Tight Pitch**
- **Al Pad- Non Reflow**



- **Interposer**
  - Polymer, Ceramic, Flex
  - Cu:Ni:Au Pad
- **Wafer**
  - Pitch limitation
- **Norm Pitch for PWB**
  - 0.5-1.27 mm

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Chip Scale Package

Pros

- Near chip size
- Testability for KGD (known Good Die)
- Ease of package handling
- Robust assembly process
  - (Grid array version)
- Die shrink or expand
- Standards
- Infrastructure
- Rework

Cons

- Limited package/assembly data availability
- Moisture sensitivity
- Thermal management
  - High I/Os
- Electrical performance
- Standards
- Routability
  - Microvia PWB for high I/Os
- Underfill?
- Reliability?
- Infrastructure?

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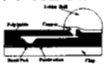
CSPs

Grid Arrays

C4

Wire Bond

Wafer



- High I/Os
- Wire bond I/O Limitation
- C4 ceramic, Wafer, Reliability?
- Assembly Robustness

Self Alignment

Leads

Leaded

No Leads

- Low I/Os
- No Leads, Reliability?
- Assembly Robustness?

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